User board design for SDLink

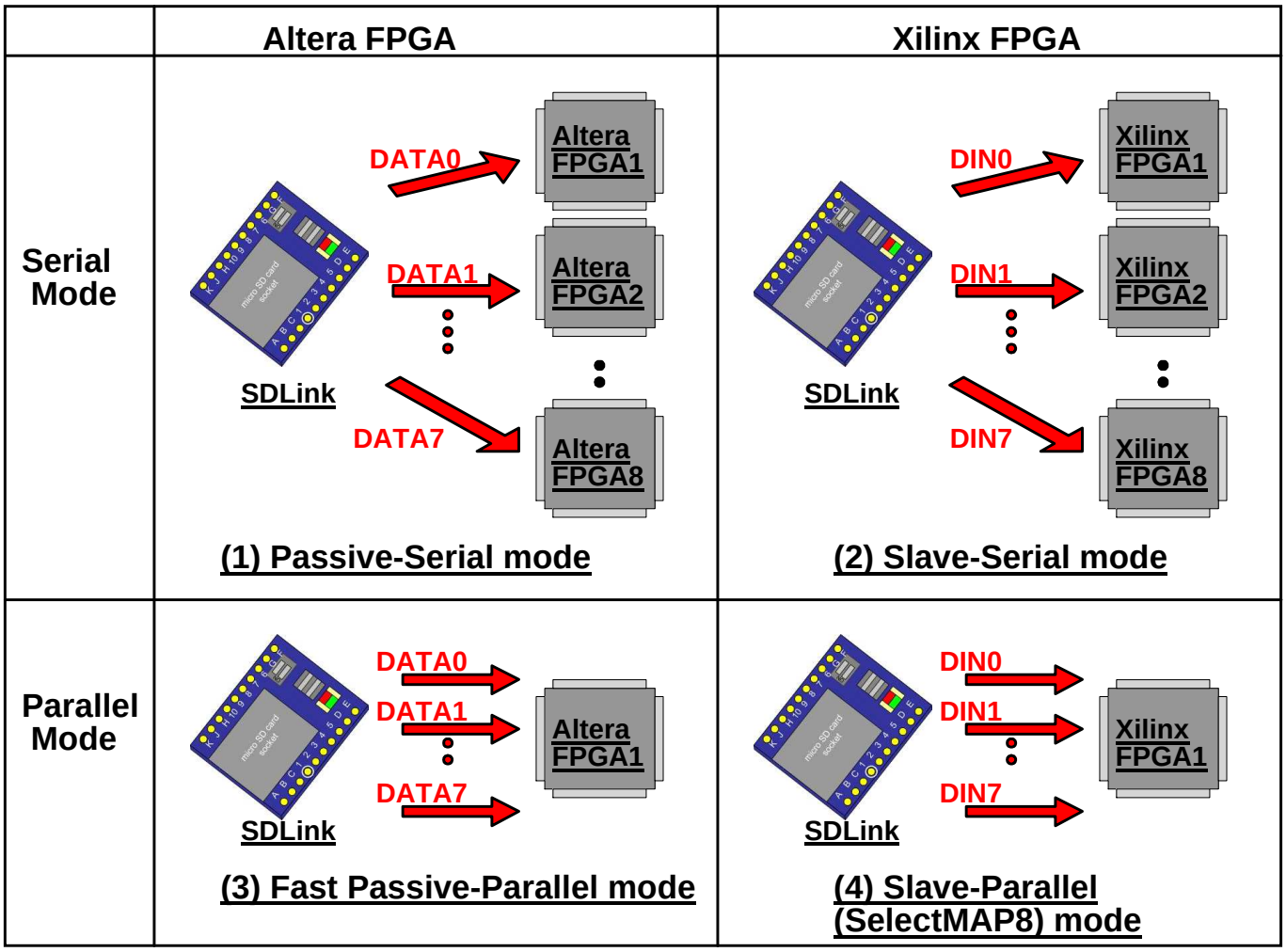
Ver2.1E 26-Aug-16

This document describes user board design guideline for FPGA configuration system using SDLink.

[Index]

1. SDLink Configuration mode

- SDLink supports following 4 types of FPGA configuration.
  - (1) Passive-Serial(PS) mode for AlteraFPGA
  - (2) Slave-Serial(SS) mode for XilinxFPGA
  - (3) Fast Passive-Parallel(FPP) mode for AlteraFPGA
  - (4) Slave-Parallel (SP / SelectMAP8) mode for XilinxFPGA
- Refer to the technical documents from FPGA vendor for more detail of each FPGA configuration mode description.
- For Stratix4 of AlteraFPGA, configuration voltage is not the 3.3V but the 3.0V. Thus consider 3.3V description part as 3.0V for Stratix4 application. (This document describes configuration power supply as VCC[Config]).

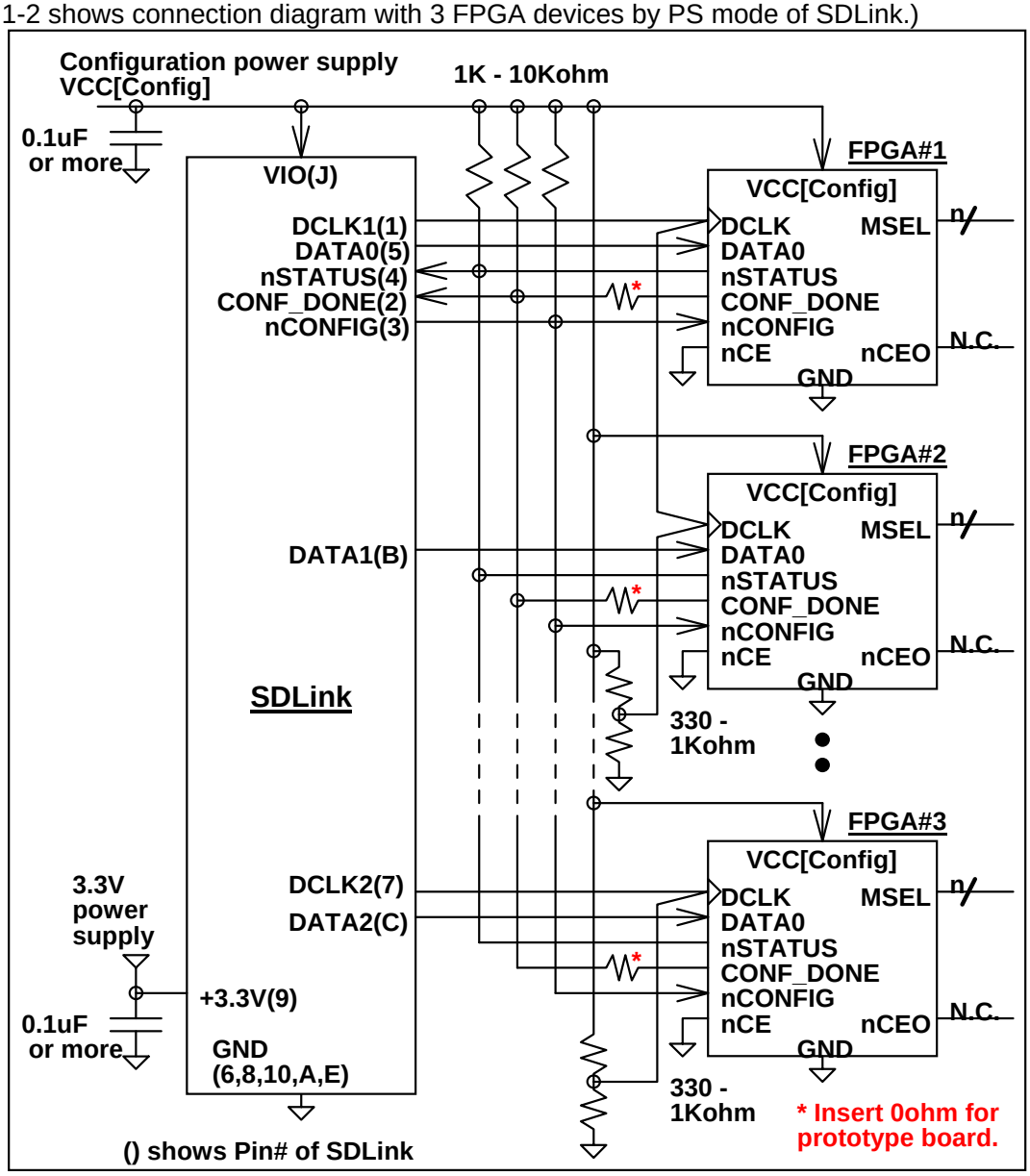


[Figure1-1] SDLink Configuration mode

- Up to 8 FPGA devices concurrent configuration is possible for serial mode of Passive-Serial and Slave-Serial.
- Only 1 FPGA device configuration is possible for parallel mode of Fast Passive-Parallel and Slave-Parallel (Select MAP8).

1.1. Passive-Serial mode for Altera-FPGA

- Build user board as figure 1-2 below for Passive-Serial configuration by Altera FPGA.
- (Figure 1-2 shows connection diagram with 3 FPGA devices by PS mode of SDLink.)

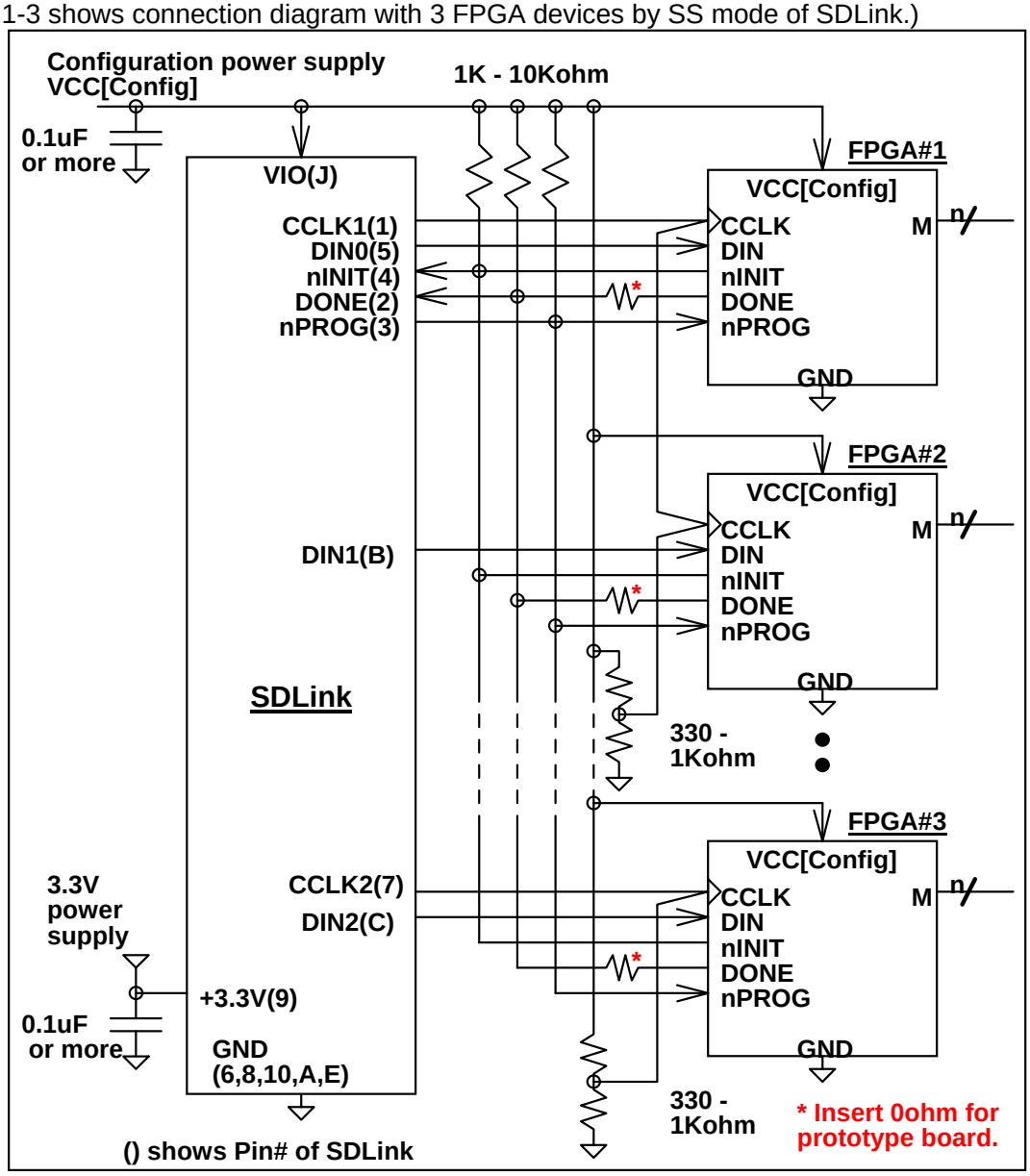


[Figure1-2] Connection diagram of PS mode by Altera FPGA

- MSEL pin settings of all FPGA must be set to PS mode.
- Set to the same power supply voltage for all FPGA configuration signal and VIO of SDLink.
- DCLK1 and DCLK2 from SDLink are identical clock signal output. Balance fan out count for each DCLK to keep signal quality.
- From DCLK1/2 output to each DCLK input of FPGA, route single stroke PCB line starting from SDLink and finish at pull-up/down (330 – 1Kohm) resistor.
- Minimize DCLK1/2 trace length.
- nSTATUS / CONF_DONE / nCONFIG should have 1K – 10Kohm pull-up resistor.
- Place bypass capacitor (0.1uF or more) adjacent to SDLink power supply pin (VIO and +3.3V).
- (*) In a prototype board, insert 0ohm resistor to CONF_DONE output of each FPGA to consider configuration troubleshooting. See “2.1. Serial mode prototype board design” section for more detail.

1.2. Slave-Serial mode for Xilinx-FPGA

- Build user board as figure 1-3 below for Slave-Serial configuration by Xilinx FPGA.
- (Figure 1-3 shows connection diagram with 3 FPGA devices by SS mode of SDLink.)

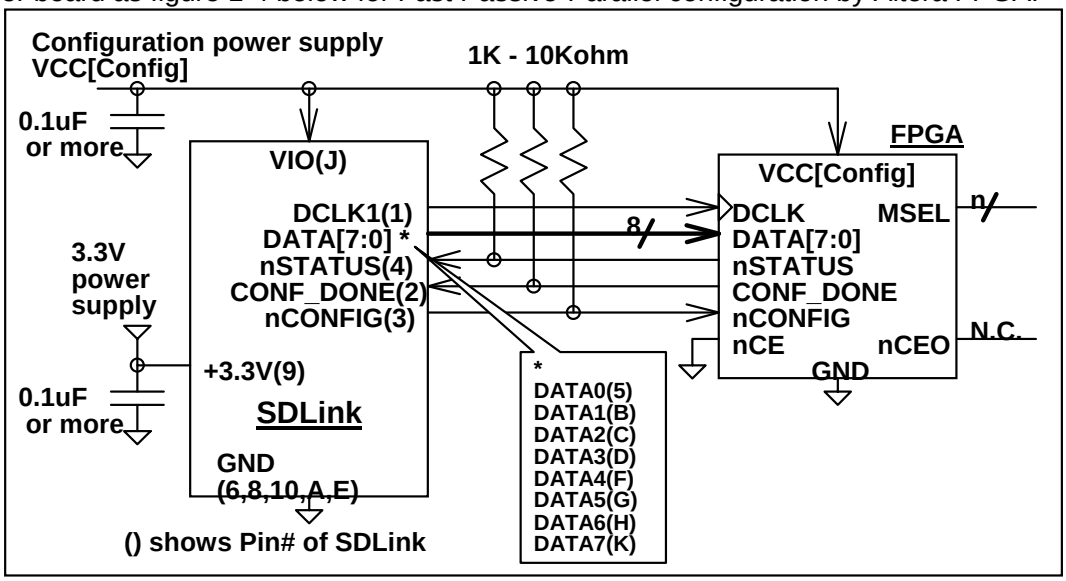


[Figure1-3] Connection diagram of SS mode by Xilinx FPGA

- M pin settings of all FPGA must be set to SS mode.
- Set to the same power supply voltage for all FPGA configuration signal and VIO of SDLink.
- CCLK1 and CCLK2 from SDLink are identical clock signal output. Balance fan out count for each CCLK to keep signal quality.
- From CCLK1/2 output to each CCLK input of FPGA, route single stroke PCB line starting from SDLink and finish at pull-up/down (330 – 1Kohm) resistor.
- Minimize CCLK1/2 trace length.
- nINIT / DONE / nPROG should have 1K – 10Kohm pull-up resistor.
- Place bypass capacitor (0.1uF or more) adjacent to SDLink power supply pin (VIO and +3.3V).
- (*) In a prototype board, insert 0ohm resistor to DONE output of each FPGA to consider configuration troubleshooting. See “2.1. Serial mode prototype board design” section for more detail.

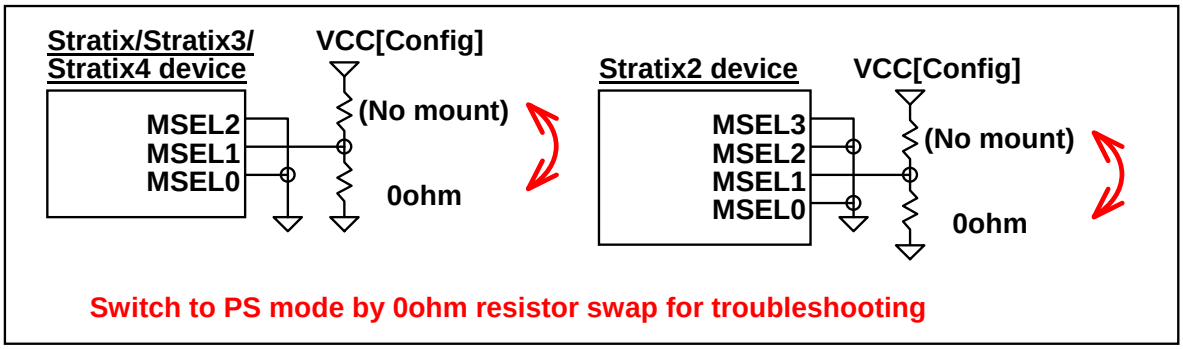
1.3. Fast Passive-Parallel mode for Altera-FPGA

- Build user board as figure 1-4 below for Fast Passive-Parallel configuration by Altera FPGA.



[Figure1-4] Connection diagram of FPP mode by Altera FPGA

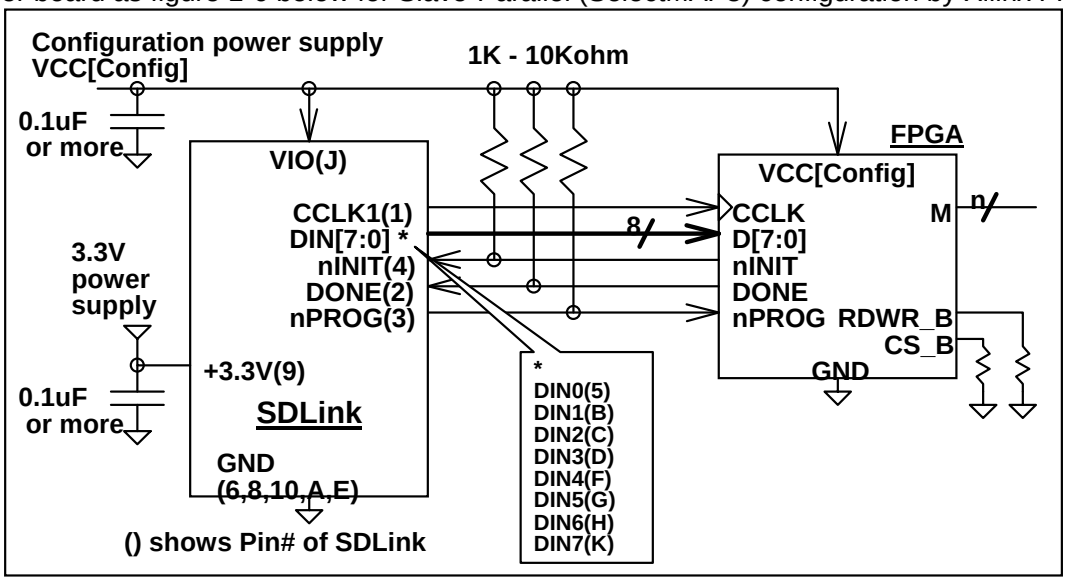
- MSEL pin settings of all FPGA must be set to FPP mode.
- Set to the same power supply voltage for all FPGA configuration signal and VIO of SDLink.
- Minimize DCLK trace length. If this length cannot be short enough, place Thevenin termination as figure1-2. User can use DCLK2 instead of DCLK1.
- nSTATUS / CONF_DONE / nCONFIG should have 1K – 10Kohm pull-up resistor.
- Place bypass capacitor (0.1uF or more) adjacent to SDLink power supply pin (VIO and +3.3V).
- DATA[7:0] output from SDLink will turn to Hi-Z state after configuration completion, so these signals are available for user circuit.
- If possible, design MSEL pin of user circuit as figure1-5 so that configuration mode can be changed between FPP and PS. In case of configuration problem occur, this board consideration can enable troubleshooting by removing SDLink from the board and try manual configuration via USB-Blaster from Quartus2 after switch configuration mode to PS.



[Figure1-5] MSEL pin connection of FPP mode

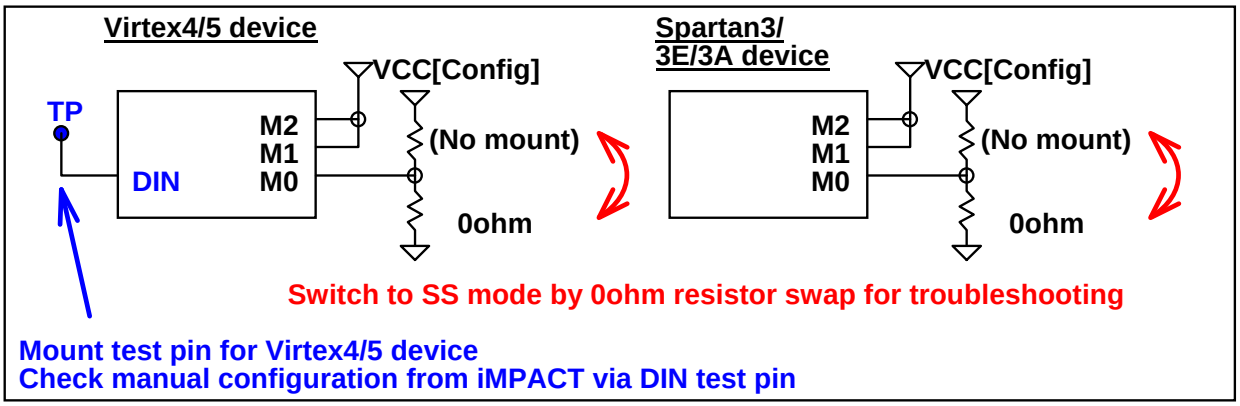
1.4. Slave-Parallel (SelectMAP8) mode for Xilinx-FPGA

- Build user board as figure 1-6 below for Slave-Parallel (SelectMAP8) configuration by Xilinx FPGA.



[Figure1-6] Connecdtion diagram of SP mode by XilinxFPGA

- M pin settings of all FPGA must be set to SP (SelectMAP8) mode.
- Set to the same power supply voltage for all FPGA configuration signal and VIO of SDLink.
- Minimize CCLK trace length. If this length cannot be short enough, place Thevenin termination as figure1-3. User can use CCLK2 instead of CCLK1.
- nINIT / DONE / nPROG should have 1K – 10Kohm pull-up resistor.
- Place bypass capacitor (0.1uF or more) adjacent to SDLink power supply pin (VIO and +3.3V).
- DIN[7:0] output from SDLink will turn to Hi-Z state after configuration completion, so these signals are available for user circuit.
- If possible, design M pin of user circuit as figure1-7 so that configuration mode can be changed between SP and SS. In case of configuration problem occur, this board consideration can enable troubleshooting by removing SDLink from the board and try manual configuration via PlatformCable from iMPACT after switch configuration mode to SS. For Virtex4/5 device, mount test pin at DIN because SS mode requires DIN pin.



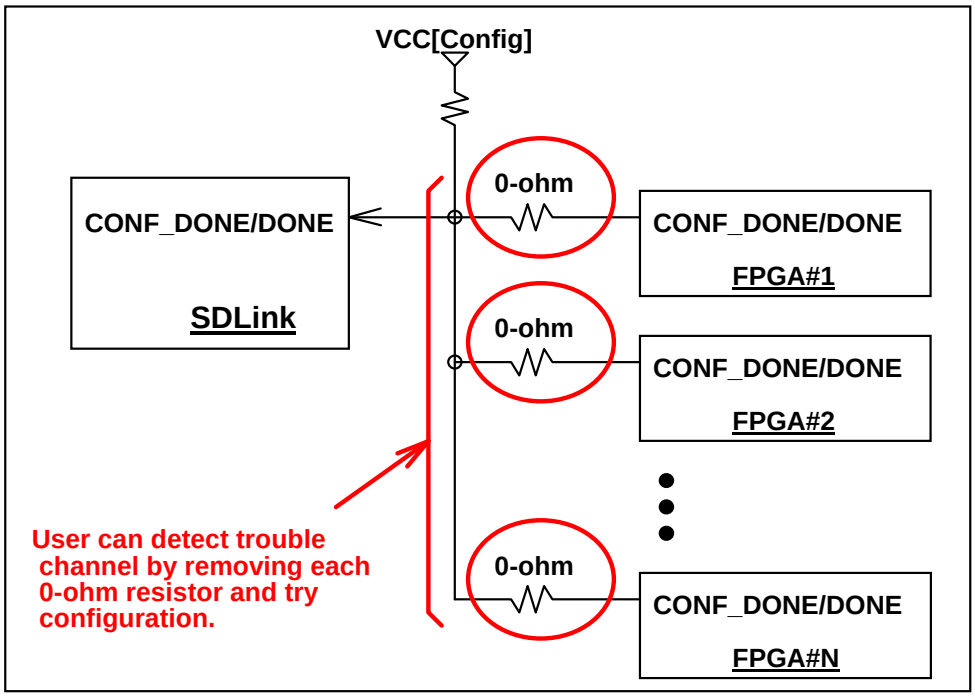
[Figure1-7] M pin connection of SP(SelectMAP8) mode

2. Recommended circuit for prototype

- When design prototype board using SDLink, add following recommendation circuit in case of configuration troubleshooting.

2.1. Serial mode prototype board design

- When design prototype board with multiple FPGA configuration circuit by SDLink, insert individual 0-ohm resistor at the signal output of CONF_DONE/DONE from each FPGA as shown in Figure2-1.
- For example if some FPGA configuration channel has a problem and cannot complete configuration, CONF_DONE/DONE output of this FPGA will keep Low drive even if all the configuration bit data is downloaded into FPGA.
- In this case, if there is no individual o-ohm resistor at CONF_DONE/DONE at each FPGA, it is impossible to detect which configuration channel has a problem because the whole this signal is driven Low by Wired-OR connection.
- With individual 0-ohm resistor, user can detect trouble channel by removing 0-ohm resistor in each channel and try configuration.



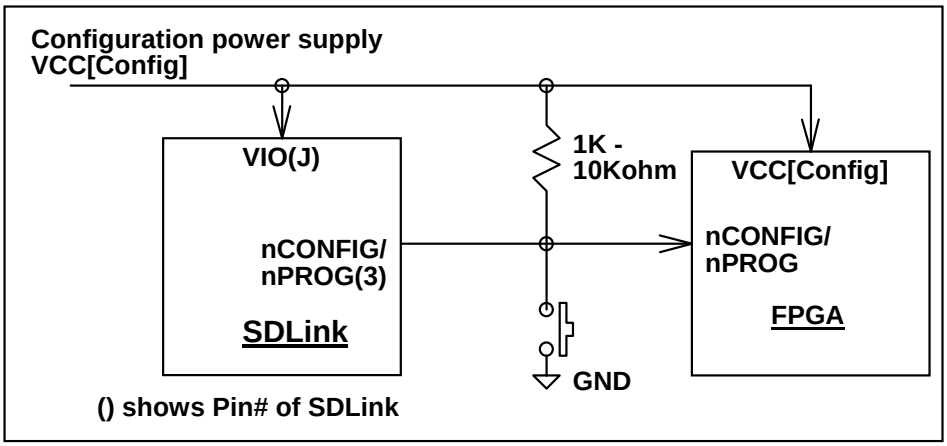
[Figure 2-1] Prototype board connection diagram of serial mode configuration

2.2. Parallel mode prototype board design

- When design prototype board of parallel mode configuration circuit by SDLink, consider circuit as figure1-5 in Altera device and figure 1-7 in Xilinx device so that user can switch to serial mode and can try manual configuration from PC in case of troubleshooting.

3. Reconfiguration by external switch

- SDLink supports reconfiguration by external switch in all configuration modes.
- Reconfiguration can be executed by force low level to nCONFIG/nPROG pin (Pin#3) by push switch.
- Place push switch between nCONFIG/nPROG pin and GND as figure 3-1 for reconfiguration circuit.



[Figure3-1] Connection diagram of reconfiguration circuit

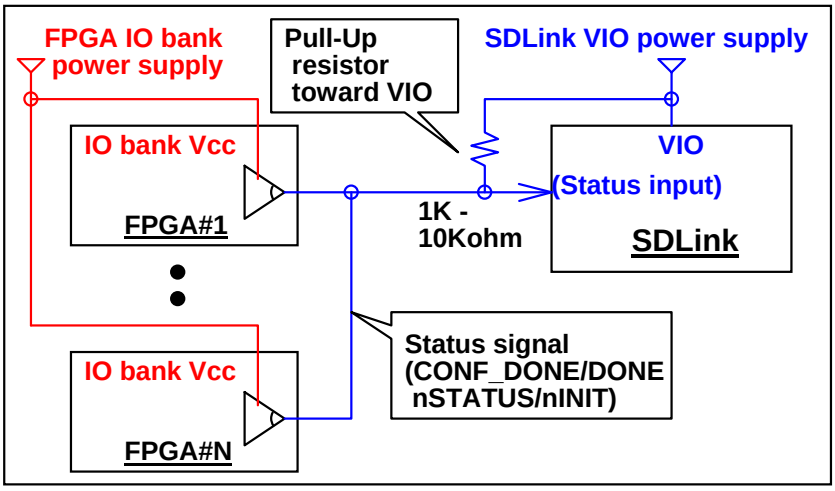
- After initial configuration at power-up, nCONFIG/nPROG pin will turn to Hi-Z state to accept external input. When SDLink detects low level to this pin, SDLink will start reconfiguration after this pin return to high level.
- Chattering protection circuit is implemented inside of SDLink so that user circuit does not require this protection circuit.
- When nCONFIG/nPROG pin is already low level at power-up, SDLink will wait this pin return to high level and then start configuration.
- When SDLink detects low level of nCONFIG/nPROG pin during configuration, SDLink will cancel configuration in progress and wait this pin return to high level, and then start configuration again.

4. Design for different configuration voltage

- Fundamentally, adjust configuration power supply voltage of SDLink (VIO) to the same voltage as IO level of DCLK/CCLK in FPGA.
- Other than the special case, DCLK/CCLK voltage level should be 2.5V or 3.3V, so that VIO should also be 2.5V or 3.3V.
- This section individually describes configuration signal design for different voltage level from clock signal when VIO is set to 2.5V or 3.3V.

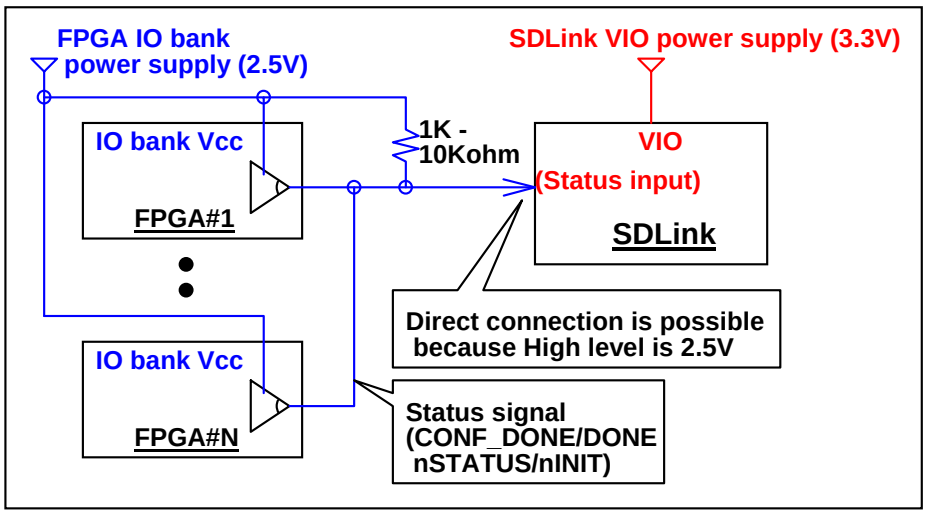
4.1. Status signals (CONF_DONE/DONE & nSTATUS/nINIT)

- Configuration status signals（CONF_DONE/DONE and nSTATUS/nINIT）are open-drain output from FPGA and are connected Wired-OR style on user board.
- When FPGA IO bank voltage of status signal is same or higher than the VIO voltage for SDLink power supply, simply mount Pull-Up resistor toward VIO as shown in Figure4-1 below.



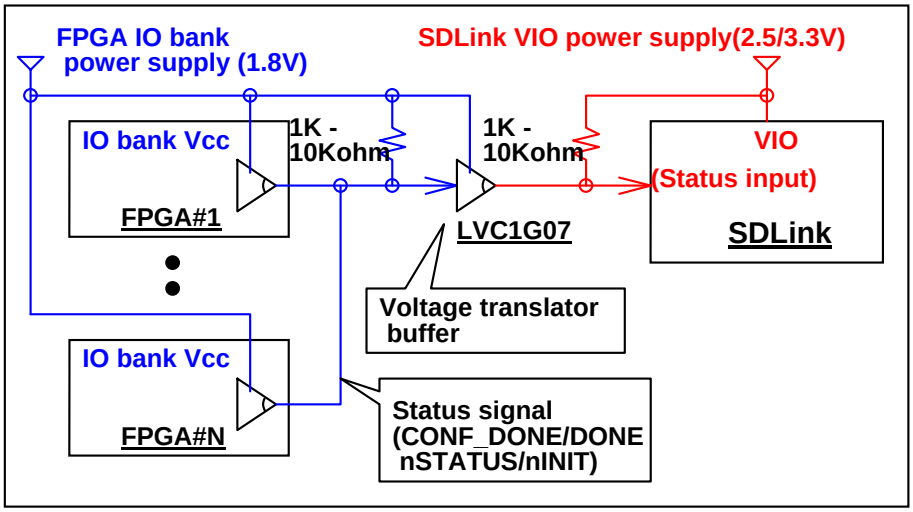
[Figure4-1] Connection diagram when IO bank voltage of status signal is higher than VIO

- When FPGA IO bank voltage of status signal is lower than the VIO voltage, and FPGA side is 2.5V and VIO is 3.3V, mount Pull-Up resistor toward 2.5V that is the power supply of FPGA IO bank as shown in Figure4-2 below. In this case, voltage translator buffer is not necessary because High level of status signal is 2.5V so that it can exceed VIH=17.V of SDLink input.



[Figure4-2] Connection diagram when IO bank is 2.5V and VIO is 3.3V case

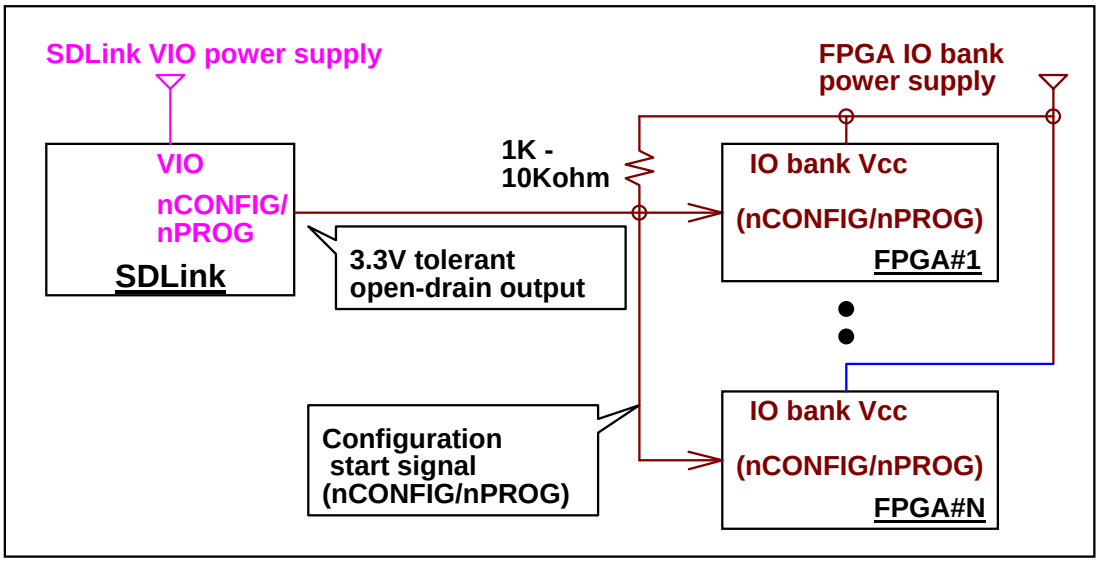
- When FPGA IO bank voltage of status signal is than the VIO voltage, and FPGA side is 1.8V and VIO is 2.5V or 3.3V, insert voltage translator buffer (such as LVC1G07 for example) into Status signal as shown in Figure 4-3 below.



[Figure4-3] Connection diagram when IO bank is 1.8V and VIO is 2.5V or 3.3V case

4.2. Start signal (nCONFIG/nPROG)

- Configuration start signal（nCONFIG/nPROG）is open-drain output from SDLink. This pin is 3.3V tolerant whichever VIO voltage is 1.8V, 2.5V, or 3.3V.
- Even when FPGA IO bank voltage of start signal input is different, voltage translator buffer is not necessary for this signal.
- Mount Pull-Up resistor toward FPGA IO bank power supply as shown Figure 4-4 below.



[Figure 4-4] Connection diagram of start signal (nCONFIG/nPROG)

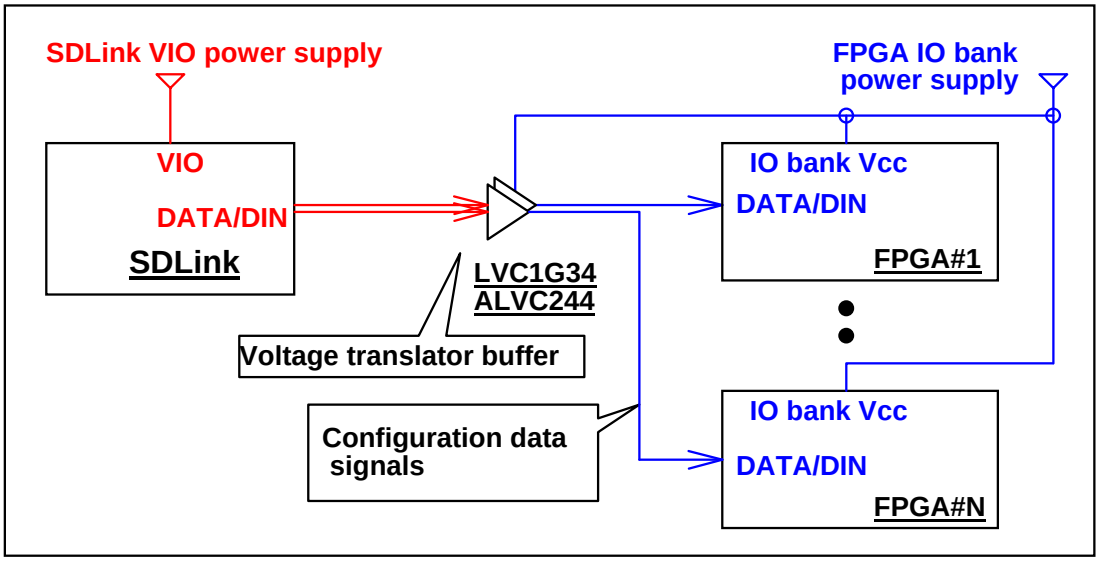
4.3. Data signals (DATA[7:0]/DIN[7:0])

- Configuration data signals（DATA[7:0]/DIN[7:0]）are PushPull type output from SDLink.
- When FPGA IO bank voltage is different from VIO of SDLink, voltage translator buffer is necessary.
- However, FPGA IO bank voltage is 3.3V and VIO voltage of SDLink is 2.5V, voltage translator buffer is not necessary because High level of output data from SDLink is more than 2.0V so that they can exceed VIH=1.7V of FPGA input.
- Figure 4-1 below shows voltage translator is necessary or not for data signals.

SDLink VIO voltage	FPGA IO bank voltage	Voltage translator
2.5V	**1.8V**	**Necessary**
2.5V	2.5V	(Not necessary)
2.5V	3.3V	(Not necessary)
3.3V	**1.8V**	**Necessary**
3.3V	**2.5V**	**Necessary**
3.3V	3.3V	(Not necessary)

[Figure4-1] Voltage translator required for data signals

- Because data signals are rather high speed so that open-drain type is not applicable to the voltage translator buffer.
- However, it is recommendable for easy design to use LVC1G24 (1 data channel case) or ALVC244 (multiple data channel case) that has 3.3V input tolerant and is high-speed device as shown Figure 4-5 below.
- When FPGA IO bank voltage is 2.5V or 3.3V, LVC244A (a little slower than ALVC244) is also applicable.



[Figure4-5] Connection diagram of configuration data (DATA[7:0]/DIN[7:0]) signals

5. Design consideration for Xilinx device

- In FPGA configuration system using SDLink, design consideration might be necessary for some device family.
- This section describes such design consideration for Xilinx device family.

5.1. Design consideration for Virtex-6

- Virtex-6 family does not support 3.3V I/O so that VIO voltage of SDLink must be set to either 2.5V or 1.8V.
- So Bank0 of Virtex-6 must be 2.5V or 1.8V, and in case of SlaveSelectMAP, also set 2.5V or 1.8V to Bank24 that include D[7:0].

5.2. Design consideration for Spartan-6

- SUSPEND pin of Spartan-6 should be tied to GND.
- When user design 1.8V to Bank2, Vccaux of Spartan-6 must not be 3.3V but be 2.5V. (Refer to ug380 for more detail.)

5.3. Design consideration for 7-Series (Virtex-7/Kintex-7/Artix-7)

- For Virtex-7, both DIN for SlaveSerial and D[7:0] for SlaveSelectMAP are located in Bank14 of HP (High Performance) Bank.
- Because HP Bank does not support 2.5V or 3.3V voltage, VIO of SDLink must be set to 1.8V.
- For Kintex-7 and Artix-7, Bank14 is assigned to HR (High Range) Bank and can support all of 3.3V, 2.5V, and 1.8V. Refer to the following figure5-1 for configuration voltage setting.

Table 2-9: **Configuration Mode, Compatible Voltages, and CFGBVS Pin Connection**

Configuration Mode	Configuration Interface I/O Voltage	Applicable Family			Compatible Bank Voltages			Required CFGBVS Pin Connection
		Artix-7 Family	Kintex-7 Family	Virtex-7 Family	Bank 0 V_{CCO_0} Voltage	Bank 14 V_{CCO_14} Voltage	Bank 15 V_{CCO_15} Voltage	
Serial, SPI, or SelectMAP	3.3V	√	√	N/A(1)	3.3V	3.3V	Any(1)	V_{CCO_0}
	2.5V	√	√	N/A(1)	2.5V	2.5V	Any(1)	V_{CCO_0}
	1.8V	√	√	√	1.8V	1.8V	Any(1)	GND

Notes:
1. In the Virtex-7 FPGA, bank 14 and bank 15 are high-performance banks limited to 1.8V or lower I/O standards.
2. JTAG interface is always supported in bank 0 at the V_{CCO_0} voltage level regardless of the configuration mode.
3. Virtex-7 HT devices support only 1.8V operation for bank 0.

Kintex-7 and Artix-7 supports all of 3.3V, 2.5V, and 1.8V configuration.

Virtex-7 only can support 1.8V configuration, so set 1.8V to both Bank0 and Bank14, and connect CFGBVS to GND.

[Figure 5-1] Configuration Voltage of 7-Series FPGA

5.4. Design consideration for UltraScale (Kintex/Virtex UltraScale)

- Configuration voltage of SlaveSerial mode
  - ✓ For UltraScale family, only Bank0 is used for SlaveSerial configuration, so that all of 3.3V, 2.5V, and 1.8V are supported in both Kintex and Virtex UltraScale family.
  - ✓ When configuration voltage is 3.3V or 2.5V, set CFGBVS to VCCO_0 (VIO of Bank0). When 1.8V, set CFGBVS to GND.

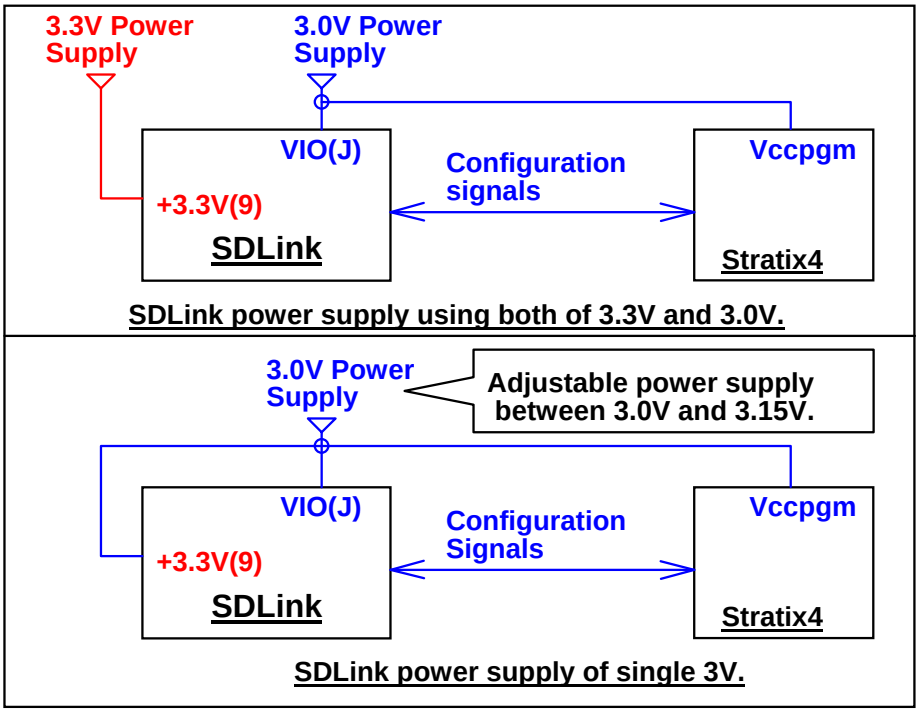
- Configuration voltage of SlaveSelectMAP mode
  - ✓ In parallel configuration mode, both Bank0 and Bank65 are used.
  - ✓ Use same power source for both Bank0 and Bank65.
  - ✓ Only 1.8V configuration is supported in KU095 and Virtex UltraScale device because Bank65 is assigned to HP Bank. (SDLink does not support 1.5V configuration.) In this case, set CFGBVS to GND.
  - ✓ Bank65 of Kintex Ultrascale except KU095 is assigned to HR Bank, so all of 3.3V, 2.5V, and 1.8V configuration are supported. When configuration voltage is 3.3V or 2.5V, set CFGBVS to VCCO_0, and when 1.8V, set CFGBVS to GND.

- Set POR_OVERRIDE pin to GND because microSD on SDLink module needs initialization time.

6. Design consideration for Altera device

6.1. SDLink power supply for StratixIV, StratixV, and ArriaV

- Because StratixIV, StratixV, and ArriaV GZ supports not the 3.3V configuration but the 3.0V configuration. user board must mount 3.0V power supply unless all the circuit operates under lower power supply of 2.5V or 1.8V only. (Note that ArriaV GX, GT, SX, and ST family supports 3.3V configuration.)
- When user board furnishes both of 3.3V and 3.0V power supply, SD power supply of SDLink (+3.3V of Pin#9) is connected to 3.3V power supply, and configuration power supply of SDLink (VIO of Pin#J) is connected to 3.0V power supply.
- However in case if all the other user circuit only use 3.0V power supply, it is not proper to prepare another 3.3V power supply only for SDLink because of additional cost and board space consumption.
- In this case, single 3.0V power supply can cover SDLink power supply on condition that real output voltage of 3.0V power supply can be adjusted to between 3.0V and 3.15V as shown figure 4-6 below.



[Figure6-1] Single 3.0V power supply for SDLink with adjustable voltage between 3.0V and 3.15V.

- Set POR delay not to Fast but to Standard. This is because microSD on SDLink needs initialization time before configuration start, and this initialization time is around 300msec so that it cannot reduce configuration time even if POR delay is set to Fast mode.
- Disable both data compression and data security feature.
- FPP data width must be 8bit. (16bit and 32bit width are not supported.)
- When Stratix V or Arria V is set to PS mode, MSEL[4:0]=(10001), and when set to FPPx8 mode, MSEL[4:0]=(11000).

6.2. Configuration mode of Cyclone IV

- SDLink only supports 3.3V or 2.5V for CycloneIV device (both GX and E), so 1.8V or 1.5V configuration is not available.
- Set POR Delay to Standard because microSD on SDLink needs initialization time before configuration start, and this initialization time is around 300msec so that it cannot reduce configuration time even if POR delay is set to Fast mode.
- For CycloneIV GX family, supported configuration mode is categorized by device size and package.
- For small CycloneIV GX device that does not support FPP mode (MSEL3 pin not exist), set MSEL[2:0]=(GND, GND, GND) to select PS mode and Standard POR Delay.
- For large CycloneIV GX device that supports FPP mode (MSEL3 pin exist), set MSEL[3:0]=(VCC,GND,GND,GND) if user selects PS mode configuration. Considering user board design complexity, FPP mode is not recommended.

Table 8–3. Configuration Schemes for Cyclone IV GX Devices (EP4CGX15, EP4CGX22, and EP4CGX30 [except for F484 Package])

Configuration Scheme	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) (1)
AS	1	0	1	Fast	3.3
	0	1	1	Fast	3.0, 2.5
	0	0	1	Standard	3.3
	0	1	0	Standard	3.0, 2.5
PS	1	0	0	Fast	3.3, 3.0, 2.5
	1	1	0	Fast	1.8, 1.5
	0	0	0	Standard	3.3, 3.0, 2.5
JTAG-based configuration (2)	(3)	(3)	(3)	—	—

For small CycloneIV GX family, set MSEL [2:0] = (GND,GND,GND)

Table 8–4. Configuration Schemes for Cyclone IV GX Devices (EP4CGX30 [only for F484 package], EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150) (Part 1 of 2)

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) (1)
AS	1	1	0	1	Fast	3.3
	1	0	1	1	Fast	3.0, 2.5
	1	0	0	1	Standard	3.3
	1	0	1	0	Standard	3.0, 2.5
PS	1	1	0	0	Fast	3.3, 3.0, 2.5
	1	1	1	0	Fast	1.8, 1.5
	1	0	0	0	Standard	3.3, 3.0, 2.5
	0	0	0	0	Standard	1.8, 1.5
FPP	0	0	1	1	Fast	3.3, 3.0, 2.5
	0	1	0	0	Fast	1.8, 1.5
	0	0	0	1	Standard	3.3, 3.0, 2.5
	0	0	1	0	Standard	1.8, 1.5

For large CycloneIV GX family, set MSEL [3:0] = (VCC,GND,GND,GND) when use PS mode

[Figure6-2] Configuration mode of CycloneIV GX when use PS mode

- For CycloneIV E family, set MSEL[3:0]=(GND,GND,GND,GND) because microSD on SDLink needs initialization time before configuration start, and this initialization time is around 300msec so that it cannot reduce configuration time even if POR delay is set to Fast mode.
- Considering user board design complexity, FPP mode is not recommended.
- For E144 and F256 package of Cyclone E family that does not have MSEL[3] pin, set MSEL[2:0]=(GND,GND,GND) so that it needs to set PS mode, 2.5V or 3.3V configuration voltage, and standard POR Delay.

Table 8–5. Configuration Schemes for Cyclone IV E Devices

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) (1)
AS	1	1	0	1	Fast	3.3
	0	1	0	0	Fast	3.0, 2.5
	0	0	1	0	Standard	3.3
	0	0	1	1	Standard	3.0, 2.5
AP	0	1	0	1	Fast	3.3
	0	1	1	0	Fast	1.8
	0	1	1	1	Standard	3.3
	1	0	1	1	Standard	3.0, 2.5
	1	0	0	0	Standard	1.8
PS	1	1	0	0	Fast	3.3, 3.0, 2.5
	0	0	0	0	Standard	3.3, 3.0, 2.5
FPP	1	1	1	0	Fast	3.3, 3.0, 2.5
	1	1	1	1	Fast	1.8, 1.5
JTAG-based configuration (2)	(3)	(3)	(3)	(3)	—	—

MSEL [3:0] = (GND,GND,GND,GND) for CycloneIV E family

[Figure6-3] Configuration mode of CycloneIV E

Revision History

Rev.	Date	Description
1.0	Mar/01/2008	Initial revision release.
1.1	Mar/04/2008	Added recommendation circuit for parallel mode to switch serial mode for troubleshooting.
1.2	Mar/13/2008	Fixed block diagram to avoid ambiguous pull-up power supply. Fixed incorrect spell.
1.3	Mar/21/2008	Added recommendation circuit of 0-ohm insertion to each (CONF)_DONE signal from FPGA for troubleshooting.
1.4	Apr/01/2008	Added design description for different configuration voltage.
1.5	Dec/02/2008	Added Stratix4 support description.
2.1E	Aug/26/2016	Added latest device description to adjust Japanese document